



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,763	09/17/2003	Kent A. Dickey	10002827-2	1746
7590 07/11/2008 HEWLETT-PACKARD COMPANY Intellectual Property Administration P. O. Box 272400 Fort Collins, CO 80527-2400			EXAMINER	
			MASKULINSKI, MICHAEL C	
			ART UNIT	PAPER NUMBER
			2113	
			MAIL DATE	DELIVERY MODE
			07/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KENT A. DICKEY and MICHAEL L. ZIEGLER

Appeal 2008-0723
Application 10/664,763
Technology Center 2100

Decided: July 10, 2008

Before JAMES D. THOMAS, LANCE LEONARD BARRY, and
STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 21-40. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

A. INVENTION

The invention at issue involves error indication in a distributed system (Spec. 4). In particular, error containment in a distributed system is accomplished by using one bit in a packet header (*id. 4*).

B. ILLUSTRATIVE CLAIM

Claim 21, which further illustrates the invention, follows:

21. A method for providing a distributed high performance coherent memory with error containment, comprising the steps of:
 - reading an error indication included in a data packet, reflective of a current state of a unit;
 - determining if said current state of said unit is in error mode;
 - permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode;
 - driving an error indicator to a subject processor if said current state of unit is in error mode; and
 - ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode.

C. REJECTION

Claims 21, 24-31, and 39 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,295,585 (“Gillett”). Claims 22, 23, and 32-38 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over U.S. Patent

No. 6,651,193 (“Dickey”). Claims 1-20 have been cancelled. The Examiner indicates allowability of claim 40 (Final Rej. 7-8).

II. CLAIM GROUPING

When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone. Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.

37 C.F.R. § 41.37(c)(1)(vii) (2005).¹

Appellants argue claims 21 and 24-31 as a first group (App. Br. 4-6) and claims 22, 23, and 32-38 as a second group (App. Br. 5-6). We select claim 21 as the sole claim on which to decide the appeal of the first group and claim 32 as the sole claim on which to decide the appeal of the second group. We decide the appeal of claim 39 separately.

¹ We cite to the version of the Code of Federal Regulations in effect at the time of the Appeal Brief. The current version includes the same rules.

III. CLAIMS 21 AND 24-31

As set forth above, we select claim 21 to decide the appeal of claims 21 and 24-31.

Appellants assert that although Gillett discloses STAE (Suppress Transmit After Error) and SRAE (Suppress Receive After Error) bits, Gillett, according to Appellants, discloses that “the STAE bit [and the SRAE bit] is not part of a packet, but rather is part of a page control table” (App. Br. 5).

The Examiner finds that Gillett discloses a Transmit Path Error (TPE) bit that “is used to indicate whether there was a Transmit Path Error” and a Receive Path Error (RPE) bit that “is used to indicate whether there was a Receive Path error” and that “the STAE and SRAE bits are used in conjunction with the TPE and RPE bits, which are transmitted in the packet” (Ans. 16). We agree with the Examiner that Gillett discloses an error indication (i.e., TPE and RPE bits) that is included in a data packet, as recited in claim 21. For example, Gillett discloses an “ACK field in the header portion of the MC packet” (col. 12, ll. 9-10) that contains a “TPE bit [that is] used to indicate whether there was a Transmit Path Error” (col. 12, ll. 42-43) and an “RPE bit [that] is used to indicate whether there was a Receive Path error” (col. 12, ll. 44-45). Because the TPE bit and RPE bit of Gillett indicate errors, we find that the TPE and RPE bits constitute “error indications.” Also, because the TPE and RPE bits are contained in an ACK field in a packet, we agree with the Examiner that the “error indications”

(i.e., TPE and/or RPE bits) are included in a data packet. Appellants do not refute this finding.

It follows that Appellants have failed to demonstrate that the Examiner erred in rejecting claim 21. We therefore affirm the rejection of claim 21, and of claims 24-31, which fall therewith.

IV. CLAIM 39

Appellants argue that “Gillett does not disclose at least this limitation [of transporting error indications together with data which is in error]” (App. Br. 5). For reasons set forth above, we agree with the Examiner that Gillett discloses error indications (i.e., TPE and/or RPE bits) that are transported together with data which is in error, as recited in claim 39.

It follows that Appellants have failed to demonstrate that the Examiner erred in rejecting claim 39. Therefore, we affirm the rejection of claim 39.

V. CLAIMS 22, 23, AND 32-38

As set forth above, we select claim 32 to decide the appeal of claims 22, 23, and 32-38.

Appellants do not refute the Examiner’s rejection. Because Appellants do not contest the merits of the double patenting rejection, we summarily sustain the Examiner’s provisional rejection of claim 32 for obviousness-type double patenting. We rule on the record that is before us.

Appeal 2008-0723
Application 10/664,763

Our affirmance of the double patenting rejection is only provisional, and “might be obviated by future events.” *See In re Wetterau*, 356 F.2d 556, 558 (CCPA 1966).

Therefore, we affirm the rejection of claim 32, and of claims 22, 23, and 33-38, which fall therewith.

VI. ORDER

In summary, the rejections of claims 21-31 and 39 under § 102(e) and of claims 22, 23, and 32-38 under the doctrine of obviousness-type double patenting are affirmed.

No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rwk

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400